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09/736,357	12/15/2000	Hideo Miyake	1614.1104	8942

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,357	MIYAKE ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Paper Nos. 2,4,5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amerson (patent No. 5,778,219) in view of Tan (patent No. 5,920,710).

3. Amerson taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Executing a second instruction prior to execution of a first instruction (i.e., speculatively)(branch instruction) where the second instruction is placed after the first instruction in a program (e.g., see col. 2, lines 16-31);

b) When an address of first data to be executed by the first instruction is included in an address region of second data to be processed by the second instruction and an exception occurs in the execution of the second instruction a buffer or tag is used to keep a record that an error has occurred and means to check when executing another execution from the same block whether the exception for any other instruction in the same block had occurred (e.g., see col. 6, lines 33-53), Amerson did not expressly detail (claim 1,9) overwriting an execution result of the first instruction data corresponding to the address of the first data. Tan, however, taught (e.g., see col. 9, lines 2-18) canceling speculative results when an exception causing instruction or

branch instruction is detected in the program wherein the exception causing or branch instruction precedes the instruction that is speculatively executed in program order.

4. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Amerson and Tan. The addition of the Tan teachings of deleting the results of the speculatively executed instruction would have reduced the amount of memory that was used in the program execution by freeing space that stored results not to be used so that those memory locations could be used later in the program in the Amerson system.

5. As to the further limitation of claims 2,3,4 Tan taught performing speculative load operations along with store operations in program order in one embodiment (e.g., see col. 12, lines 21-36). Tan also taught canceling instructions including speculative instructions when a branch was mispredicted (e.g., see col. 11, lines 6-19, and col. 26, line14-col. 27, line 47). Therefore, clearly, when the instruction (including a load instruction) would have been cancelled the results would have been canceled, such as taught by Tan with respect to speculative results namely, when an exception causing or branch instruction preceded an instruction that was speculatively executed (e.g., see col. 9, lines 2-18) One means to cancel the result clearly would have been to rewrite or erase the results.

6. As per claim 5, since Tan taught canceling the instructions as discussed above, it would have been obvious to one of ordinary skill that the canceling of the instruction would have been implemented as erasing the addresses or pointers to the instructions or results, or erasing the actual instructions or both. However one of ordinary skill would

have been motivated to erase the addresses to the canceled instruction or results so that the system would not erroneously use those addresses later in the processing.

7. As per claim 6, Amerson taught storing an identification of the context that was detailed as basic blocks that are crossed when crossing the boundary of a branch instruction as represented in a dependency graph (e.g., see col. 5, line 39-67, and col. 6, lines 32-65).

8. As per claim 7,8,13,14,15,16 Amerson taught the processing of the exception including the canceling of the result performed in accordance with an interrupting program which would have included instruction to perform the operations (e.g., see col. 15, lines 4-65). Therefore the processes, including the overwriting operation in the Amerson and Tan system, would have been performed by an interrupting or branching program.

9. As to the further limitation of claims 10, Tan taught performing speculative load operations along with store operations in program order in one embodiment (e.g., see col. 12, lines 21-36). Tan also taught canceling instructions including speculative instructions when a branch was mispredicted (e.g., see col. 11, lines 6-19, and col. 26, line14-col. 27, line 47). Therefore, clearly, when the instruction (including a load instruction) would have been cancelled the results would have been canceled, such as taught by Tan with respect to speculative results namely, when an exception causing or branch instruction preceded an instruction that was speculatively executed (e.g., see col. 9, lines 2-18) One means to cancel the result clearly would have been to rewrite or erase the results.

10. As per claim 11, Tan taught storage destination memory units that store the information specifying the storage units in which an address of the second data and result obtained by the executing the second instruction is stored (e.g., see col. 3, line 42-col. 4, line 35)

As per claim 12, Amerson taught storing an identification of the context that was detailed as basic blocks that are crossed when crossing the boundary of a branch instruction as represented in a dependency graph (e.g., see col. 5, line 39-67, and col. 6, lines 32-65).

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 17,18,31,32,45,51 are rejected under 35 U.S.C. 102(b) as being anticipated by Amerson (patent No. 5,778,219).

13. Amerson taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Executing a second instruction prior to execution of a first instruction (i.e., speculatively)(branch instruction) where the second instruction is placed after the first instruction in a program (e.g., see col. 2, lines 16-31);

b) When an address of first data to be executed by the first instruction is included in an address region of second data to be processed by the second instruction and an exception occurs in the execution of the second instruction a buffer or tag is used to keep a record that an error has occurred and means to check when performing another execution from the same block whether the exception for any other instruction in the same block had occurred (e.g., see col. 6, lines 33-53),

c) Inhibiting and retaining an exception operation when necessity of the exception operation is detected in the step of executing (e.g., see col. 6, lines 42-53);

d) Performing the exception operation when the retained exception operation is needed in execution of an instruction at a branch destination selected through the execution of the branch instruction (e.g., see col. 14, line 24-col. 15, line 48); and

e) Returning to the program so as to continue the execution of the instruction at the branch destination when the exception operation is finished (e.g., see col. 15, lines 36-57).

14. As to the break operation claimed in claim 45,51 as understood, this operation performs the same operation as the operation to break or change processing execution to process the exception and then returning to the processing of the program, this operation is taught by Amerson (e.g., see col. 6, lines 33-53 and col. 15, lines 36-57).

Claim Rejections - 35 USC § 103

15. Claims 19-30,33-44,46-50,52,53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amerson as applied to claims 17,18,31,32,45,51 above, and further in view of Tan (patent No. 5,920,710).

16. As per claims 19,20,21,27,34,35,39,40,41,46,48,52,54 Amerson taught when an address of first data to be executed by the first instruction is included in an address region of second data to be processed by the second instruction and an exception occurs in the execution of the second instruction a buffer or tag is used to keep a record that an error has occurred and means to check when performing another execution from the same block whether the exception for any other instruction in the same block had occurred (e.g., see col. 6, lines 33-53), Amerson also taught the processing of the exception including the canceling of the result performed in accordance with an interrupting program which would have included instruction to perform the operations in accordance with stored notification of an exception and associated data (e.g., see col. 15, lines 4-65).

17. As per claims 22,23,25,26,28,29,33,34,36,37,42,43,47,49,50,53,55,56 Tan also taught canceling instructions including speculative instructions when a branch was mispredicted (e.g., see col. 11, lines 6-19, and col. 26, line14-col. 27, line 47). Amerson taught the processing of the exception including the canceling of the result performed in accordance with an interrupting program which would have included instruction to perform the operations (e.g., see col. 15, lines 4-65). Further as per claim 24,30,38,44 from the above the processes, including the overwriting operation in the Amerson and Tan system, would have been performed by an interrupting or branching program.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Talcott (6,615,343) disclosed a DP system comprising mechanism for delivering precise exceptions in an out-of-order processor (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER

March 13, 2004